UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/889,730	10/22/2001	Peter Dominke	10191/1923	8707

26646	7590	03/08/2004

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EXAMINER
BONZO, BRYCE P

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 03/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

-- *The MAILING DATE of this communication appears n the cover sheet with the corresp ndence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 October 2001*.

2a)☐ This action is **FINAL.**   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-36* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19,22-27 and 30-33* is/are rejected.

7)☒ Claim(s) *20,21,28,29 and 34-36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☒ All b)☐ Some * c)☐ None of:

      1.☒ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

NON-FINAL OFFICIAL ACTION

Status of the claims

Claims 1-8 have been cancelled via Pre-Amendment.

Claims 19, 22-27 and 30-33 are rejected under 35 USC §102(b).

Claims 20, 21, 28, 29 and 34-36 are objected to while containing allowable matter.

Formal Matters relating to PCT

The Pre-Amendment included with PCT/DE00/00157 is acknowledged.

The search report with references is acknowledged.

Rejections under 35 USC §102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 19, 22-27 and 30-33 are rejected under 35 U.S.C. 102(b) as being

anticipated by Böhl (*The Fail-Stop Controller AE11*).

As per claim 19, Böhl discloses:

A control unit for controlling a safety-critica.1 application, the control unit comprising:

microcomputer (Figure 4, CPU);

monitoring unit including a first arrangement for measuring a quiescent current of the microcomputer (page 571 §5: Particularly the I_{DDQ}-Test structures are inserted after the first symbols pass by specifically tailored tools), and including a second arrangement for applying a test data input signal, for processing test data output signals and for comparing a corresponding test data output signal of the microcomputer to a corresponding test data output signal of the monitoring unit (Page 571 §5: Modules under logic stuck-at BIST and I_{DDQ}-Test.);

at least one quiescent current handshake line running between the first arrangement and the microcomputer for controlling the measuring of the quiescent current (Figure 4, run_iddq);

at least one test data signal transmission line running between the second arrangement and the microcomputer (Figure 4: run_bist); and

peripheral circuits (Figure 4, TAP).

As per claim 22, Böhl discloses:

The control unit of claim 19, wherein: the first arrangement includes an IDDQ measuring circuit, a voltage supply, an IDDQ measuring run control, and a control system of the monitoring unit (Figure 6);

the at least one quiescent current handshake line includes two handshake lines

running from the IDDQ measuring run control to the microcomputer (Figure 4,

run_iddq); and

at least one voltage supply line running from the voltage supply to the

microcomputer, at least one of the at least one voltage supply line running through the

IDDQ measuring circuit (Figure 6, $V_{DD\text{-}virtual}$).

As claim 23, Böhl discloses:

The control unit of claim 20, wherein the first arrangement includes an

initialization circuit for receiving an initialization signal from the voltage source after the

control unit is switched on (Figure 6: T_{bypass}), and for subsequently transmitting an

enable signal to the IDDQ measuring run control to enable an IDDQ measurement

(Figure 6: T_{Test}).

As claim 24, Böhl discloses:

The control unit of claim 19, wherein:

the second arrangement includes a test data signal generator for applying the

test data input signal to the microcomputer (§3.3), a response generator for processing

the test data input signal and for forming the corresponding test data output signal

(§3.3), a test data register for receiving the test data input signal and for transmitting the

corresponding test data output signal(§3.3) and a comparator for comparing the

corresponding test data output signal of the microcomputer to the corresponding test

data output signal of the monitoring unit (§3.3),

and the at least one test data transmission line runs between the test data

register of the second arrangement and the microcomputer (Figure 4: run_bist and

start_bist).

As claim 25, Böhl discloses:

The control unit of claim 24, wherein the at least one test data transmission line

includes two test data transmission lines (Figure 4: run_bist and start_bist).

As claim 26, Böhl discloses:

The control unit of claim 24, wherein the second arrangement includes a trigger

generator for determining an instant at which the corresponding test data output signal

of the microcomputer is available at the comparator, the microcomputer being error-free

(bist_ok is a control signal).

As claim 27, Böhl discloses:

The control unit of claim 24, wherein the second arrangement includes an error

counter for counting an error if at least one of the following is satisfied: the

corresponding test data output signal of the microcomputer, is not consistent with the

corresponding test data output signal of the monitoring unit; and the corresponding test

data output signal of the microcomputer is available at the comparator at a different

instant than one determined by the trigger generator (§3.2 In this way... 100% reliability, Figure 4: error flag).

As claim 30, Böhl discloses:

A method for testing a microcomputer of a control unit for controlling safety-critical applications, the control unit including the microcomputer, a monitoring unit, and peripheral circuits., the method comprising:

measuring a quiescent current of the microcomputer, the measuring of the quiescent current being controlled by the monitoring unit (page 571);

exchanging at least one handshake signal between the microcomputer and the monitoring unit (Figure 4, run_iddq);

applying a test data input signal to the microcomputer (§3.3);

determining a first test data output signal (§3.3); and

comparing a second test data output signal. of the microcomputer to the first test data output signal of the monitoring unit (§3.3).

As claim 31, Böhl discloses:

The method of claim 30, wherein a quiescent current measurement corresponds to an IDDO measurement (§3.4 ¶3).

As claim 32, Böhl discloses:

The method of claim 31, wherein the IDDQ measurement is performed after the control unit is switched on after being enabled by an enable signal (Figure 4: T_{Test}).

As claim 33, Böhl discloses:

The method of claim 31, wherein the second test data output signal of the microcomputer is compared to the first test data output signal of the monitoring unit while the control unit is operating (§3.3).

Allowable Matter

Claims 20, 21, 28, 29 and 34-36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant is reminded that this indication of allowable matter may be vacated should the claims be amended to in a manner which broadens the scope of the claims. The italicized portions of the claims below overcome the prior art when viewed as a whole with the remaining claim limitations.

As per claims 20 and 21:

The control unit of claim 19, wherein:

the first arrangement includes an IDDQ measuring circuit, a voltage supply, an IDDQ measuring run control, and a control system of the monitoring unit;

the at least one quiescent current handshake line includes two handshake lines

running from the IDDQ measuring run control to the microcomputer;

the first arrangement and the microcomputer are coupled by the two handshake

lines and at least one voltage supply line running from the voltage supply to the

microcomputer; and

at least one of the at least one voltage supply line runs through the IDDQ

measuring circuit.

As per claim 28:

The control unit of claim 27, wherein there is a plurality of response thresholds

for use with the error counter, and a different reaction results by exceeding each

response threshold of the plurality of response thresholds results.

As per claim 29:

The control unit of claim 25, wherein the first arrangement includes an

initialization circuit for receiving an initialization signal from the voltage source after the

control unit is switched on, for subsequently synchronizing the monitoring unit with the

microcomputer, and for then activating the test data signal generator and the error

counter.

As per claim 34:

The method of claim 31 *wherein a clock generator is stopped by the microcomputer during at least one of:* the IDDQ measurement, and the comparing of the second test data output signal of the microcomputer with the first test data output signal of the monitoring unit.

As per claims 35 and 36:

The method of claim 31, wherein *the test data input signal of the monitoring unit is generated by a test data signal generator via a feedback shift register.*

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bryce P Bonzo whose telephone number is (703) 305-4834. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Bryce P Bonzo
Examiner
Art Unit 2114

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